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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/077,947	02/20/2002	Hideki Okuyama	8039-1001	3041

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EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/077,947	OKUYAMA, HIDEKI	
	Examiner	Art Unit	
	Trisha Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 22-36 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 22-24, 26-28, 30-32, and 34-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Shibata (5,442,755).

As to claim 22, Shibata teaches a multiprocessor system comprising: a plurality of processors (processors 1, 2, 5') which send and receive predetermined information to and from each other; a shared memory (MS 4) which is shared and accessed by each of said plurality of processors; and an access manager (arbitration unit 32 or the whole storage controller 3) which manages access to said shared memory by each of said plurality of processors, wherein, when said plurality of processors are in contention to access said shared memory, said access manager selects one of said plurality of processors and permits said one of said plurality of processors to access said shared memory, wherein, once each of said plurality of processors has accessed said shared memory, when said one of said plurality of processors updates a predetermined data in said shared memory (e.g. performing fetch/store/lock setting/release by processor 1), said one of said plurality of processors requests others of said plurality of processors to access said updated

predetermined data from said shared memory (e.g. processor 1 issues a store and lock release command to thereby notify other processors so that other processor e.g. processor 2 can start its fetch/store/lock request to the updated memory) (Figs 1 and 5, and col. 4 lines 13-64 and col. 5 lines 14-33).

As to claim 23, Shibata further teaches said one of said plurality of processors requests others of said plurality of processors to update said updated predetermined data from said shared memory (e.g. processor 1 issues a store and lock release command to thereby notify other processors so that other processor e.g. processor 2 can start its fetch/store/lock request to the updated memory) (Figs 1 and 5, and col. 4 lines 13-64 and col. 5 lines 14-33).

As to claim 24, Shibata further teaches said one of said plurality of processors requests others of said plurality processors to update the predetermined data in said shared memory, when said others of said plurality of processors have not yet updated said predetermined data (e.g. processor 1 issues a store and lock release command to thereby notify other processors so that other processor e.g. processor 2 can start its fetch/store/lock request to the updated memory) (Figs 1 and 5, and col. 4 lines 13-64 and col. 5 lines 14-33).

As to claim 26, Shibata teaches a multiprocessor system comprising: a plurality of processors (processors 1, 2, 5') which send and receive predetermined signal to and from each other; a shared memory (MS 4) which is shared and accessed by each of said plurality of processors; and a contention determiner (arbitration unit 32 or the whole storage controller 3) which detects whether said plurality of processors are in contention

to access said shared memory, and permits one of said plurality of processors to access said shared memory, wherein, once said one of said plurality of processors has accessed said shared memory said one of said plurality of processors outputs an access-request signal to another one of said plurality of processors, so as to request said another one of said plurality of processors to access said shared memory, and wherein once each of said plurality of processors has accessed said shared memory, when said one of said plurality of processors updates a predetermined data in said shared memory , said one of said plurality of processors outputs re-read request signal to another of said plurality of processors, so as to request said others of said plurality of processors to access said updated predetermined data from said shared memory (e.g. processor 1 issues a store and lock release command to thereby notify other processors so that other processor e.g. processor 2 can start its fetch/store/lock request to the updated shared memory, and after processor 2 is done, it can signal other(s) to start their requests to access the shared memory, and so on) (Figs 1 and 5, and col. 4 lines 13-64 and col. 5 lines 14-33).

As to claim 27, Shibata further teaches said one of said plurality of processors outputs an update-request signal, so as to request said others of said plurality of processors to update said updated predetermined data from said shared memory (e.g. processor 1 issues a store and lock release command to thereby notify other processors so that other processor e.g. processor 2 can start its fetch/store/lock request to the updated memory) (Figs 1 and 5, and col. 4 lines 13-64 and col. 5 lines 14-33).

As to claim 28, Shibata further teaches said one of said plurality of processors outputs an update-request signal, so as to request said others said plurality processors to

update the predetermined data in said memory, when said others of said plurality of processors have not yet updated said predetermined data (e.g. processor 1 issues a store and lock release command to thereby notify other processors so that other processor e.g. processor 2 can start its fetch/store/lock request to the updated memory) (Figs 1 and 5, and col. 4 lines 13-64 and col. 5 lines 14-33).

As to claims 30, 34 and 35, Shibata teaches a shared-memory controlling method to be executed multiprocessor system including plurality of processors (processors 1, 2, 5') which send and receive predetermined information to and from each other, a shared memory (MS 4) which is shared and accessed by each of said plurality of processors, and an access manager (arbitration unit 32 or the whole storage controller 3) which manages access to said shared memory by each of said plurality of processors, said method comprising: selecting one processor of said plurality of processors, and permitting said one processor to access said shared memory, when said plurality of processors are in contention for said shared memory; performing a first access to said shared memory using said one processor (e.g. performing fetch/store/lock setting/release by processor 1); requesting others of said plurality processors to perform a second access to said shared memory, when said performing the first access to said shared memory has been done; and performing the second access to said shared memory using said others of said plurality of processors, wherein, once each of said plurality of processors has accessed said shared memory, said one processor updates a predetermined data in said shared memory and requests said others of said plurality of processors to access said updated predetermined data from said shared memory (e.g. processor 1 issues a store and lock release command

to thereby notify other processors so that other processor e.g. processor 2 can start its fetch/store/lock request to the updated shared memory, and after processor 2 is done, it can signal other(s) to start their requests to access the shared memory, and so on) (Figs 1 and 5, and col. 4 lines 13-64 and col. 5 lines 14-33).

As to claim 31, Shibata further teaches wherein said requesting step includes said one processor requesting others to update said updated predetermined data in said shared memory (e.g. processor 1 issues a store and lock release command to thereby notify other processors so that other processor e.g. processor 2 can start its fetch/store/lock request to the updated memory) (Figs 1 and 5, and col. 4 lines 13-64 and col. 5 lines 14-33).

As to claim 32, Shibata further teaches wherein said requesting step includes said one processor requesting others to update the predetermined data said shared memory (e.g. processor 1 issues a store and lock release command to thereby notify other processors so that other processor e.g. processor 2 can start its fetch/store/lock request to the updated memory) (Figs 1 and 5, and col. 4 lines 13-64 and col. 5 lines 14-33.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 25, 29, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata (5,442,755) in view of Azevedo et al. (6,496,890) (hereinafter Azevedo).

As to claims 25, 29 and 33, the argument above for claims 22, 26 and 30 applies. However, Shibata does not explicitly disclose when predetermined period time has elapsed without being selected by said access manager, said one of said plurality of processors requests others of said plurality of processors and said access manager to perform a predetermined reset operation for resetting themselves. Hauck teaches bus hang prevention wherein when a predetermined period of time has elapsed and a request from a control master is not selected by an access manager, resetting all devices on the shared bus (at least col. 2 line 60 to col. 3 line 33 and col. 7 lines 41-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include bus hang prevention wherein when a predetermined period of time has elapsed and a request from a control master is not selected by an access manager, resetting all devices on the shared bus as taught by Azevedo in the system of Shibata to prevent a permanent bus hang condition and to allow recovery of the system to a known state such as reset state (col. 7 lines 41-56).

4. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata (5,442,755) in view of Mogul (6,704,798).

As to claim 36, Shibata teaches a shared-memory controlling method comprising: selecting one processor of a plurality of processors, and permitting said processor to access a shared memory shared by the plurality of processors (processors 1, 2, 5'), when the plurality of processors are contention for the shared memory (MS 4); performing a first access to said shared memory using one processor (e.g. performing fetch/store/lock

setting/release by processor 1); requesting others of said plurality processors to perform a second access said shared memory, when the first access has been done; performing the second access to said shared memory using the others of said plurality of processors; wherein, once each of said plurality of processors has accessed shared memory, when said one processor updates a predetermined data in said shared memory in performing the first access, said one processor requests said others of said plurality of processors to access said updated predetermined data from said shared memory (e.g. processor 1 issues a store and lock release command to thereby notify other processors so that other processor e.g. processor 2 can start its fetch/store/lock request to the updated memory) (Figs 1 and 5, and col. 4 lines 13-64 and col. 5 lines 14-33). However, Shibata does not explicitly disclose the method is contained within a data signal embedded in a carrier wave representing an instruction sequence. Mogul teaches implementing a data signal embedded in a carrier Wave representing an instruction sequence (col. 14, lines 4-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method via a data signal embedded in a carrier wave representing an instruction sequence as taught by Mogul in the system of Shibata to allow the method to be stored and executed in a distributed fashion over the network.

Response to Arguments

5. Applicant's arguments filed 04-25-05, regarding "the processors of ALAIWAN et al. are never in contention" (see pages 11-12 of the Remarks) have been fully considered and are

persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art(s).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha Vu whose telephone number is 571-272-3643. The examiner can normally be reached on Mon-Thur and alternate Fri 8:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu
Examiner
Art Unit 2112

uv

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